10/02/02

Errata: CS4202 Rev. A2

(Reference CS4202 Data Sheet revision DS549PP1)

Functional Problems

General issues

1. If power is removed and re-applied, the reference may not start up if the analog supply has decayed below 2.0 V but has not been fully discharged. In PLL mode this will also prevent the clocks from running. After removing power from the device it should not be powered up again until the analog supply voltage has dropped below 400 mV.

   This issue should not cause any problems since the supply voltages usually discharge very quickly, so under real world use scenarios the failure condition would not occur.

2. DAC performance is slightly degraded in the left channel and greatly degraded in the right channel if DSA=11 (output slots 10/11 are selected) and VRA=1 (SRC is enabled).

   Output slots 10/11 are commonly used for dedicated S/PDIF data only, so this problem would not occur under normal circumstances.

3. During ATE test mode, the weak pulldown resistors on BIT_CLK and SDATA_IN are active.

   This problem would only be observed if ATE test mode is entered, which is usually done during production test or debug activities. It does not affect normal operation.

Powerdown issues

4. In PLL mode, asserting PR3+PR4+PR5 will not shut down the digital logic and the clocks. Software can circumvent this problem by asserting PR2+PR4+PR5 instead when trying to achieve maximum power savings in PLL mode. This problem does not affect the other clocking modes.

   Software workaround possible in driver.

Performance Problems

Pops and clicks

5. Clearing PR1 causes a click if the DAC path is unmuted. Software can prevent this problem by muting the PCM Out Volume (reg 18h) (if DDM=0) or muting the Master Out Volume (reg 02h), Headphone Volume (reg 04h) and Mono Out Volume (reg 06h) (if DDM=1) before clearing PR1.

   Software workaround possible in driver.

Analog performance

6. The MIC1/2 inputs show increased distortion above -5 dBV (0.55 Vrms) input voltage.

   This problem does not occur with the microphone boost (any setting except 0 dB) enabled. PC 99 and PC 2001 THD+N compliance testing is usually done with the microphone boost enabled, so this problem will not affect real world performance or certification.

Current consumption

7. In XTAL mode, the digital supply current (DVdd) is too high during RESET (0.8 mA).

   This problem cannot be addressed due to the current clocking mode detection scheme.

8. The analog supply current (AVdd1) is too high during PR3 (1.5 mA).

   This problem cannot be addressed due to the current anti-pop scheme.

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